What is claimed is :

1. A symbol timing recovery circuit, utilized in a phase demodulator, generating phase differences at the same sampling points of neighboring symbols to determine an optimal sampling point in a symbol period, comprising:

a phase difference generating circuit for first mapping the phase difference to a first quadrant of a phase plane, subtracting the mapped difference by a default phase value to obtain a result and taking a square of the result;

a selection circuit connected to the phase difference generating circuit for outputting the result of a phase difference of every sampling point of a symbol to its corresponding output end;

an accumulation module including accumulators whose number is equal to the number of the sampling points in a symbol, said accumulators receiving the outputs of the selection circuit for accumulating phase differences of the same sampling points of continuous neighboring symbols; and

a comparison module for comparing the sums of phase differences outputted from the accumulators; the optimal sampling point corresponding to an accumulator having the smallest sum of the phase differences.

2. The symbol timing recovery circuit of Claim 1, wherein the default phase value is $\pi/4$.

3. The symbol timing recovery circuit of Claim 1, wherein said selection circuit is a demultiplexer.

4. The symbol timing recovery circuit of Claim 1, wherein each of the symbols has 25 sampling points which means that a sampling rate is 25 times of a symbol rate.

5. A symbol timing recovery circuit, utilized in a phase demodulator to generate phase differences at the same sampling points of neighboring symbols to determine an optimal sampling point in a symbol period, comprising:

a phase difference generating circuit for mapping the phase difference to a first quadrant of a phase plane, subtracting the mapped difference by a default phase value to obtain a result and taking a square of the result;

an operation circuit for summing up the squared result of phase differences of the same sampling points of neighboring symbols;

a delay circuit module including a plurality of delay circuits whose number is equal to the number of sampling points in a symbol; wherein the delay circuits are connected in series, and the output of the last delay circuit cooperates with the operation circuit to generate an input to a first delay circuit; and

a comparison module for comparing the sums of phase differences outputted from the delay circuit module to determine an optimal sampling point corresponding to a delay circuit generating the smallest sum of the phase differences.

6. The symbol timing recovery circuit of Claim 5, wherein the default phase value is $\pi/4$.

7. The symbol timing recovery circuit of Claim 5, wherein said operation circuit is an adder.

8. The symbol timing recovery circuit of Claim 5, wherein the symbol has 25 sampling points which means that a sampling rate is 25 times of a symbol rate.

9. A symbol timing recovery method, utilized in a phase

demodulator to generate phase differences at the same sampling points of neighboring symbols to determine an optimal sampling point in a symbol period, comprising the following steps:

mapping a phase difference to a first quadrant of a phase plane;

subtracting the phase difference mapped to the first quadrant by a default phase value to obtain a result, and taking a square of the result;

computing phase differences of every sampling point in a symbol, and accumulating phase differences at the same sampling points of the continuous neighboring symbols; and

determining a sampling point having the smallest sum of the phase differences, thereby obtaining an optimal sampling point.

10. The symbol timing recovery method of Claim 9, wherein the default phase value is $\pi/4$.

11. The symbol timing recovery method of Claim 9, wherein the symbol has 25 sampling points, which means that a sampling rate is 25 times of a symbol rate.